Digital optical fiber link

Features

- *Battery operated digital link with 2.5 V, 3.3 V or 5 V input / output levels*

- *CRC-5 protection on every transmitted data frame*

- *2 or 4 digital channels per link*

- *Sample rate of 5 MSa/s per channel*

- *Designed for EMC test labs with optical signal isolation*

- *Short-circuit protected digital outputs*



Product description

EMCgear Digital optical fiber link EFL-D is a range of products for isolating digital signals between two locations, especially in EMC test laboratories.

Two or four channels transfer sampled logic states at 5 MSa/s. **Independent input and output voltage options of 2.**5 V, 3.3 V and 5 V support logic-level translation.

FPGA-based communication applies CRC validation to every data frame. The receiver monitors link validity and controls the digital outputs.

The link uses aluminum housings and filtered electrical interfaces. Optical fiber separates the Input and Output units without an electrical signal connection.

Technical parameters

General

Channels *)	*2 or 4*
Signal type	*Digital logic*
Input / output logic levels *)	*2.5 V* / 3.3 V / 5 V *Input and output selected separately*
Sample rate	*5 MSa/s per channel*
Input impedance / capacitance	*100 kOhm / 27 pF*
Input filter cutoff	*10.6 MHz*
Battery	*4.2 V / 5000 mAh*
Operating time	*Typ. 20 hours*
Operating temperature	*0 to 55 °C*

*) Variant dependent. See list of available variants.

Use case

Each EFL-D digital fiber link consists of an Input side and an Output side.

As connection medium can be used SMA-905 terminated optical fiber, widely accepted within standard EMC test types of equipment.

Following example scenarios can be used:

a) Input side is placed inside EMC test chamber to monitor DUT during the test.

b) Output side is place inside EMC test chamber to stimulate DUT during the test.

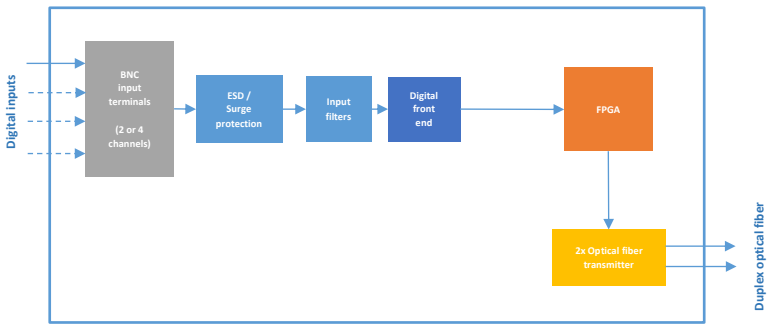
c) Both sides can also be used on the test table to isolate DUT logic signals from monitoring or stimulation equipment.



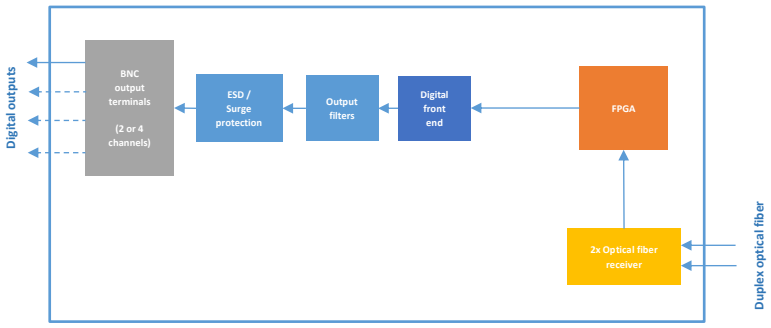
INPUT SIDE OUTPUT SIDE

Function block diagram

Input side



Output side



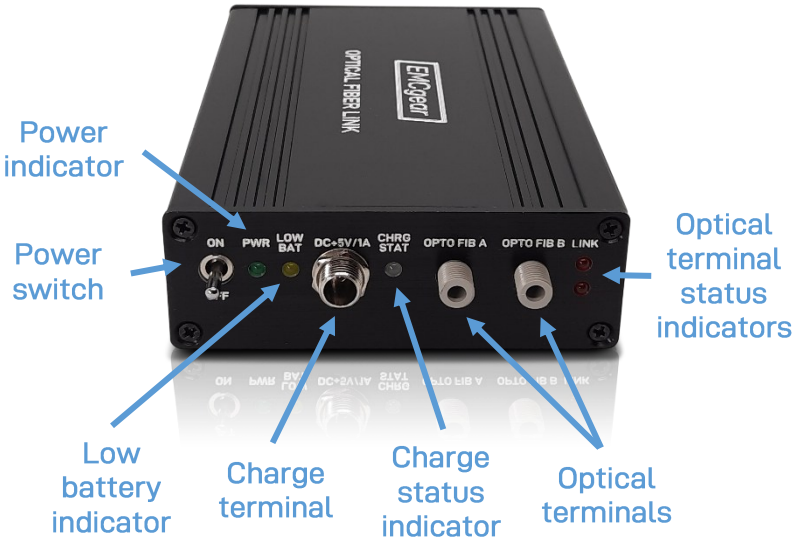
Front side terminals



2 - 4 digital input or output terminals

*) Variant and link side dependent. See list of available variants.

Back side terminals



Quick start guide

1.) **Check the serial numbers and EFL-D variant codes** on both the Input and Output **side before connection.**

Use a matched device pair. Confirm the channel count, input logic level and output logic level against the DUT and connected equipment.



2.) **Interconnect both devices with crossed duplex optical fiber with corresponding parameters.**
See chapter Technical parameters for details about optical interface.

3.) **Power on both Input and Output side with marked toggle switch.**

4.) **The digital fiber link is ready for functional checks. Verify logic states at the outputs before starting the test.**



Normal operation

Normal operation is initiated immediately after both link sides are powered on (power switch in ON state). Optical fiber have to be properly connected between both nodes.
The receiver qualifies the received data before enabling normal operation. Startup and qualification timing must be validated on EFL-D hardware.

The LINK indicator on the Output side indicates the qualified receiver state. The Input side LINK indicator shows transmitter readiness.
After link qualification, sampled digital inputs are reproduced at the corresponding outputs using the selected output logic level.



Connection problems

A missing or erroneous optical connection is indicated by an inactive LINK indicator on the Output side. CRC-5 checks each received frame; the receiver also supervises the rate of valid frames.
Check the fiber connections and inspect or replace the optical cable. Verify the intended low output state during loss of communication before use.

*) Please note that input side LINK indicator remains always active even with disconnected optical fiber. This indicate that input side is ready to establish connection with output side (optical transmitters are properly driven)



Battery status indication

Low battery pre-warning is indicated with solid yellow light on corresponding link side.
When LOW BAT is active, charge the device promptly.



Fully drained battery brings device into disabled state (indicated with disabled PWR indicator on the corresponding link side).
With the link disabled, digital outputs are intended to be driven LOW.



Remote battery status monitoring

EFL-D device offers special function for **remote monitoring of the "Input side" battery status**.
This can be especially useful during EMC tests, when Input side is placed inside anechoic chamber or out of sight of test operator.
The remote battery status is carried in the protected data payload. The Output side LINK indication can flash with a 1 s period; status polarity must be validated for the released firmware.



Charge status indication

After plugging in external charger into marked DC jack terminal charge process begins immediately. Ongoing charge process is indicated with solid red light on the CHRG STAT indicator.

Finished change process is indicated with solid green light and remains in this state until charger is removed or battery voltage drops below recharge level.





Charge while device is powered on

If necessary, EFL-D devices can be continuously charged during normal operation.
A linear charging circuit is used in the EFL-D platform. EFL-D emissions during charging require validation with the intended power supply and cable arrangement.
Use a power supply with the voltage, current and polarity specified on the EFL-D unit. Maintain the required isolation and verify the EMC test setup with charging connected.

Please note, in this mode CHRG STAT indicator always shows "Charge in progress" with solid red light (charge done indication is disabled).



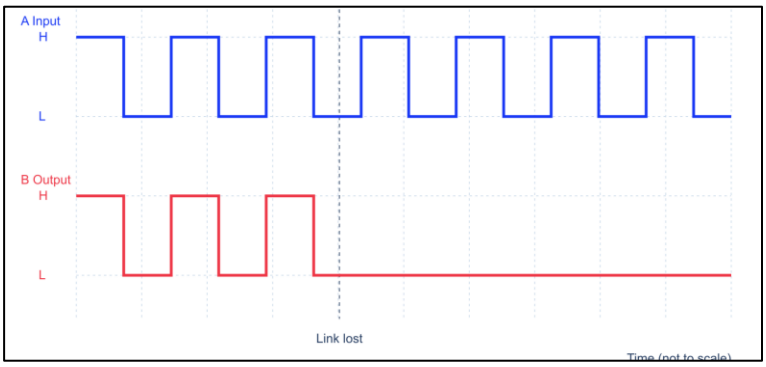
Signal integrity control

Every transmitted channel-data frame is covered by real-time CRC calculation

Scenario no. 1)

Loss of transmission link communication

Illustration of optical link removal: input A continues to toggle; output B enters the intended LOW state after the receiver detects loss of valid communication. Timing is illustrative.

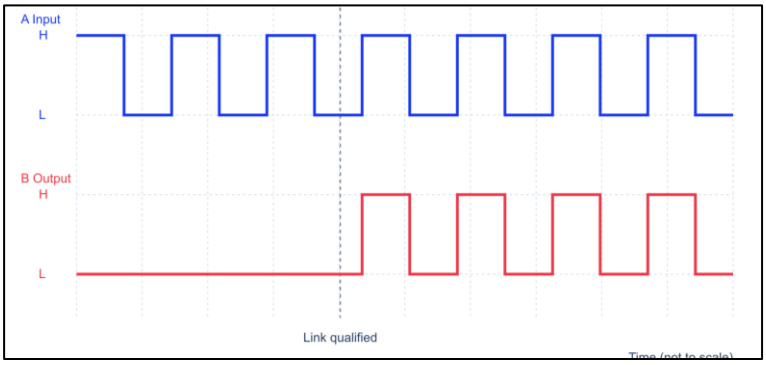


BLUE A = Input; RED B = Output

Scenario no. 2)

Communication recovery

Illustration of recovery: the receiver requalifies the optical link and resumes propagation of sampled digital states. Timing is illustrative.

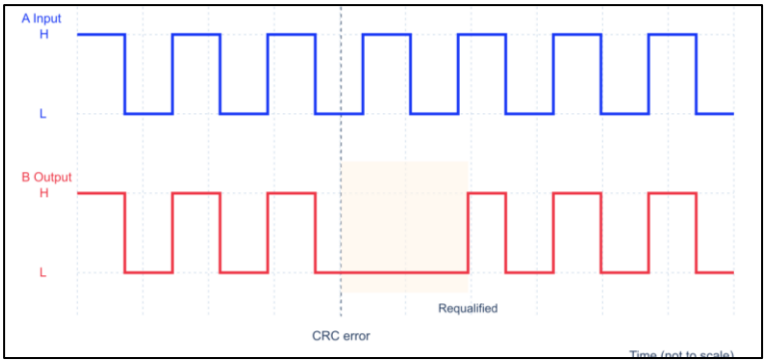


BLUE A = Input; RED B = Output

Scenario no. 3)

Single communication error (injected error)

Illustration of a CRC error during transmission. The input remains a digital square wave.
The intended output response includes link supervision and requalification.



BLUE A = Input; RED B = Output

Technical parameters

Optical interfaces

Optical fiber terminals	*2x SMA-905 jack*
Optical transmitter wavelength	*820 nm*
Recommended optical fiber type	*1x duplex or 2x simplex*
Recommended optical fiber structure	*50 / 125 µm or 62.5 / 125 µm (core / cladding)*
Recommended optical fiber length	*0 to 900 m*

Transmission link

Data rate	*Typ. 50 Mbit/s*
Data integrity protection	*CRC-5 on every data frame*
Datalink initialization time	*TBD*
Sample rate	*5 MSa/s per channel 2 or 4 channels*

Digital inputs

Input impedance	*100 kOhm*
Input capacitance	*27 pF*
Input filter cut-off frequency	10.6 MHz
Input logic levels	*2.5 V / 3.3 V / 5 V*
ESD rating (as per IEC 61000-4-2)	*± 15kV (air) ± 8 kV (contact)*
Surge protection (as per IEC 61000-4-5, 8/20 *µs)*	*12 A*

Digital outputs

Output impedance	*100 Ohm*
Output logic levels	*2.5 V / 3.3 V / 5 V*
Short-circuit protection	*Yes*
Output current / overload limit	*± 25 mA*
ESD rating (as per IEC 61000-4-2)	*± 15kV (air) ± 8 kV (contact)*
Surge protection (as per IEC 61000-4-5, 8/20 *µs)*	*12 A*

Digital interface notes

Input / output timing

5 MSa/s sampling

The 10.6 MHz input filter cutoff is not the guaranteed toggle frequency. Minimum pulse width, propagation delay, jitter and input thresholds remain to be characterized.

Battery

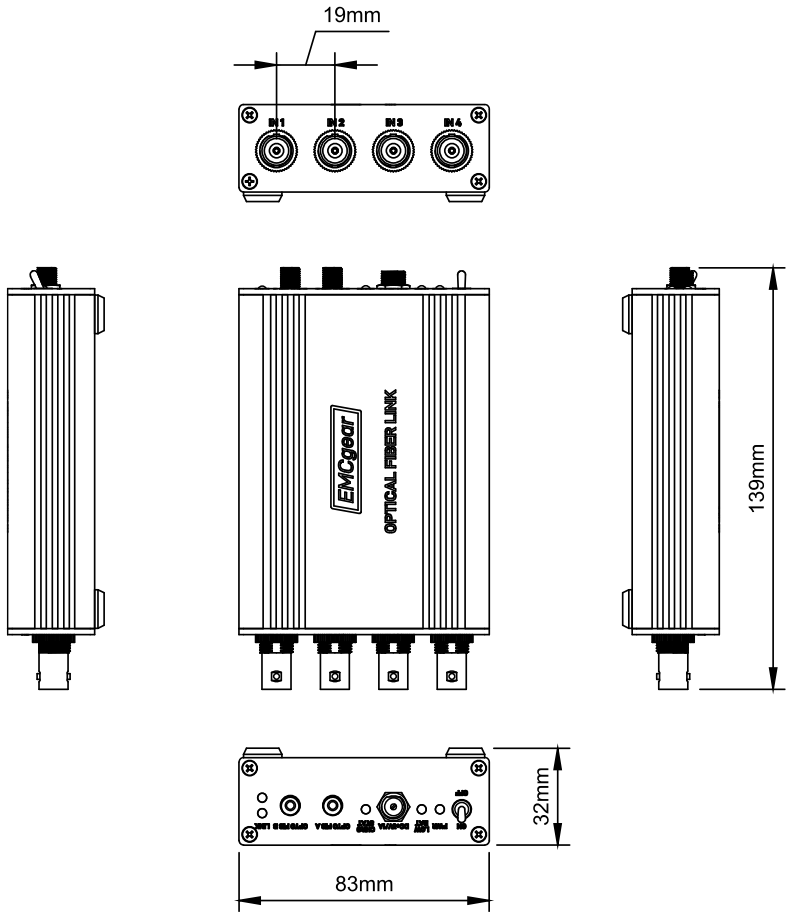
Battery type	1 cell LiPo battery
Battery charge voltage	*4.2 V*
Battery capacity	*Nom. 5000 mAh*
Battery protection circuit	*Overcharge and deep undercharge protection*
Battery life cycle	*Min. 500 full charge cycles*
Battery replacement	*Replacement battery kit available, ask for further information.*

Charging

Charge current	*Typ. 1000 mA*
Charge time	*Max. 6 hours (from discharged to fully charged status)*
Operating time	*Typ. 20 hours (on fully charged battery)*
Charging terminal *)	*DC jack 5.5 / 2.1 mm with screw terminal, center pin positive (5/16-32 UNEF 2A thread)*
External charger voltage *)	*5.0 to 6.0 V DC*
External charger rating *)	*Min. 3 A*

*) See list of recommended accessories for suitable wall charger.

Mechanical dimensions



*) Mechanical dimensions for INPUT and OUTPUT side are equal.

Scope of delivery
(per EFL-D link kit)

EFL-D Digital fiber link – Input side box	*1 pc*
EFL-D Digital fiber link – Output side box	*1 pc*
Foam lined transport box (330 x 272 x 82 mm)	*1 pc*

Warranty

2-year manufacturer warranty

Conformity

Conform with EMC Directive 2014/30/EU

EN 61326-1 IEC 61000-4-2 IEC 61000-4-3 IEC 61000-4-5 IEC 61000-4-6	

Variant list	Description	Order code
4-channel link	Channels: 4 Input/output range: 0 to 2.5V (log 0 / log 1) Sample rate: 5 MSa/s	EFL-D-25-25-4
	Channels: 4 Input/output range: 0 to 3.3V (log 0 / log 1) Sample rate: 5 MSa/s	EFL-D-33-33-4
	Channels: 4 Input/output range: 0 to 2.5V (log 0 / log 1) Sample rate: 5 MSa/s	EFL-D-50-50-4
2-channel link	Channels: 2 Input/output range: 0 to 2.5V (log 0 / log 1) Sample rate: 5 MSa/s	EFL-D-25-25-2
	Channels: 2 Input/output range: 0 to 3.3V (log 0 / log 1) Sample rate: 5 MSa/s	EFL-D-33-33-2
	Channels: 2 Input/output range: 0 to 2.5V (log 0 / log 1) Sample rate: 5 MSa/s	EFL-D-50-50-2

Recommended accessories

	Description	Order code
Charger adaptor	**Power Adaptor 100-240V to 5V 3A 2.1mm** Screw Lock UK/EU/US/AU plug (Mfg. no. : Brainboxes PW-500)	**EFL-A-AD1** (2 pcs are recommended)
Fiber patch cables	**Fiber patch cable SMA905-SMA905 10m** Duplex fiber Termination: 2x SMA905 on both ends Optical mode: OM1, Cladding: 62.5/125 µm Length: 10m	**EFL-A-FPC10**
	Fiber patch cable SMA905-SMA905 20m Duplex fiber Termination: 2x SMA905 on both ends Optical mode: OM1, Cladding: 62.5/125 µm Length: 20m	**EFL-A-FPC20**

Draft release checks

CRC implementation

CRC-5 verified in EFLD_CRC_SLAVE.vhd: 5-bit LFSR, polynomial x^5 + x^2 + 1, reset state 11111. Project file includes this module.

Receiver payload mapping

EFLD_SPI_SLAVE checks payload bits 9:5, but the top module maps output bits from 4:0. The receive register is also read after further shifting. Resolve this mismatch and validate output behavior before release.

Parameters to validate

Confirm input thresholds and maximum voltage, output drive current, delay and minimum pulse width, short-circuit limits, optical reach, battery runtime and EMC ratings. Variant codes are draft allocations; verify manufacturable combinations.